Confirmation No. 9412

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	HIJZEN	Examiner:	Duong, Khanh B.
Serial No.:	10/538,217	Group Art Unit:	2822
Filed:	June 9, 2005	Docket No.:	NL021418 US
Title:	METHOD OF MANUFACTURE OF A TRENCH-GATE SEMICONDUCTOR DEVICE		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 23, 2007 and in response to the rejections of claims 1-2, 4-6 and 8-10 as set forth in the Final Office Action dated July 17, 2007.

Please charge Deposit Account number 50-0996 (NXPS.239PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017021/0932 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-2, 4-6 and 8-10 stand rejected. Claims 3 and 7 are indicated as reciting allowable subject matter, and claims 11-16 are allowed. Accordingly, claims 1-2, 4-6 and 8-10 are presented for appeal. Complete listings of the claims under appeal and the allowed and allowable claims not under appeal are provided in separate Appendices to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action entered on August 30, 2007.

V. Summary of Claimed Subject Matter

Appellant's claims recite trench gate semiconductor devices and methods of manufacturing trench gate semiconductor devices.

Independent claim 1 recites a method of manufacturing a trench gate semiconductor device (see generally Figs. 1a-1e and accompanying discussion). The steps recited in the method are: providing a silicon device body having a first major surface (see, for example, silicon device body 1 in Fig. 1a), the silicon device body having a drain region of a first conductivity type (see, for example, drain region 4 in Figs. 1a-1e) and a body region over the

drain region (see, for example, body layer 6 in Figs. 1a-1e); forming a trench extending downwards into the silicon device body from the first major surface (see, for example, trench 8 in Fig. 1a), the trench having sidewalls (see, for example, sidewalls 28 in Fig. 1a) and a base (see, for example, base 29 in Fig. 1a); etching the silicon at the base of the trench to form porous silicon at the base of the trench (see, for example, specification paragraph [0028], and porous silicon 26 in Fig. 1b); thermally oxidizing the device to oxidize the porous silicon at the bottom of the trench (see, for example, specification paragraph [0030]) to form a plug at the base of the trench (see, for example, oxidized porous silicon plug 30 in Fig. 1c); and depositing conductive material within the trench to form a gate (see, for example, polysilicon gate 34 in Fig. 1d).

Independent claim 9 recites a trench MOSFET (see, for example, specification paragraphs [0034] through [0037], and Fig. 1e) that includes: a drain region of first conductivity type (see, for example, drain region 4 in Figs. 1a-1e); a body region over the drain region (see, for example, body layer 6 in Figs. 1a-1e); a trench extending from a first major surface through the body region (see, for example, trench 8 in Fig. 1a); source regions of the first conductivity type laterally adjacent to the trench at the first major surface (see, for example, source diffusion 14 in Fig. 1e); thermal gate oxide on the side walls of the trench (see, for example, oxide 12 in Fig. 1e on the side walls 28 indicated in Figs. 1a-1c); a gate electrode in the trench (see, for example, polysilicon gate 34 in Fig. 1d) insulated from the body region by the gate oxide; characterized by a thick oxide plug formed of oxidized porous silicon at the base of the trench extending into the drain region (see, for example, oxidized porous silicon plug 30 in Fig. 1c).

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 9 and 10 stand rejected under 35 U.S.C. § 102(b) over Murphy (U.S. Patent No. 6,444,528).

2. Claims 1-2, 4-6 and 8 stand rejected under 35 U.S.C. § 103(a) over Murphy in view of Lynch *et al.* (U.S. Patent No. 4,643,804).

VII. Argument

1. The 102(b) rejection of claims 9 and 10 should be overturned because the Examiner improperly disregards claim elements clearly not disclosed by Murphy.

A rejection under 35 U.S.C. § 102(b) cannot be sustained if the cited reference does not teach or suggest all the elements recited in the claims. In attempting to support the Section 102(b) rejection, the Examiner has not called out each claim element and argued for its correspondence in the applied reference, providing specific citations. Rather, the Examiner has attempted to find correspondence between the Murphy reference and Appellant's claims by subtraction – conveniently disregarding recitations in Appellant's claims that are inarguably not present in the Murphy reference. Specifically, the Examiner argues that the claim 9 phrase, "a thick oxide formed of oxidized porous silicon," is a product-by-process limitation that bears no patentable weight, and can therefore be disregarded. Appellant requests a Board decision finding that the Examiner has improperly disregarded language in the claims, and overturning the 102(b) rejection of claims 9-10.

Patent applicants commonly use process-like language to recite structural elements without having such language relegated to product-by-process status. The Federal Circuit recently stated, "even words of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and by default interpreted in their structural sense, unless the patentee has demonstrated otherwise." *See 3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365 (Fed. Cir. 2003), finding that the terms "embossed" and "multiple embossed" were structural limitations and not product-by-process limitations. *See also Hanzai v. United States Int'l Trade Comm'n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997), concluding that "chemically engraved" was not a process term. The M.P.E.P. confirms that a patent application is permitted to use structural language that recites a process, and instructs the Examiner to give such language due consideration:

> The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive

structural characteristics to the final product. M.P.E.P. § 2113; *See, also, In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

Despite the Examiner's assertions to the contrary, claim 9 is not a product-by-process claim, and the cited language cannot be disregarded as a product-by-process limitation. Claim 9 clearly recites a thick oxide plug formed of oxidized porous silicon, not a thick oxide plug formed by oxidizing porous silicon. The claim specifies what the plug is made of (*i.e.*, oxidized porous silicon), not the process by which the plug is made. Appellant submits that the phrase "oxidized porous silicon" is customarily used in the art to refer to a structure as opposed to a process. Indeed, a cursory search reveals that over twenty patents have issued in the United States in the past thirty years that use the term "oxidized porous silicon" as a structural recitation in the claims.

Appellant further submits that a process limitation can be used in the claim to recite oxidizing a porous silicon plug, and the limitation would still carry patentable weight because it would impart distinctive structural characteristics on the final product (*i.e.*, oxidation). As such, disregarding the phrase from patentability analysis is wholly improper.

Appellant submits that the rejection cannot stand in view of the claims properly interpreted to include structural consideration of "oxidized porous silicon." The Murphy reference does not teach or suggest that the bottom layer of the gate dielectric contains silicon that is both oxidized and porous. For at least these reasons, the rejection should be reversed.

2. The 103(a) rejection of claims 1-2, 4-6 and 8 should be overturned because the Examiner has failed to present a proper reason for the combination in light of contrary teachings in the references.

The Supreme Court recently acknowledged that, "[a] patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007). As such, to state a *prima facie* case of obviousness, there must be some valid reason to make the combination or modification that is not contrary to the teachings of the references. In this regard, the Supreme Court further noted:

> [I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.
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> *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007)

In this case, the Examiner's purported reason to combine the references is not valid because (a) the primary Murphy reference already presents an adequate solution, and (b) the Examiner derives the purported reasoning from the problems presented in the secondary Lynch reference without evidence that the primary Murphy reference presents those problems. Appellant therefore requests that the Board overturn the 103(a) rejection for failure to state a *prima facie* case of obviousness.

The Examiner concedes that Murphy does not disclose forming a plug at the base of a trench by etching to form porous silicon and thermally oxidizing the porous silicon to form the plug. Instead, the Examiner looks to the teachings of Lynch to cure the deficiencies of the Murphy reference. However, Murphy already provides a thick dielectric layer at the base of a trench by selective deposition. As such, Appellants submit that one of skill in the art would have no reason to look for another way to provide a thick dielectric layer in the trench of Murphy.

The Examiner asserts that one of skill in the art would combine Murphy with Lynch in order to "minimize the stress level in the plug region and improve the electrical characteristics of trenches that include bottoms having surface roughness and/or sharp or irregular corners" as taught by Lynch. However, the Examiner fails to establish that the Murphy reference is susceptible to these problems. Moreover, the Examiner has not presented any evidence that modifying Murphy with the cited teaching of Lynch would in any way minimize the stress level in the plug region of the Murphy reference, which is different from the plug region of the Lynch reference.

The cited portions of the Lynch reference teach that surface roughness 20 and/or sharp or irregular corners (22 and 24) are a problem when a thin dielectric layer 18 (*e.g.*, 200 Å) is grown or deposited on the bottom of the trench 10. *See, e.g.*, Figure 1 and Col. 2:40-68. However, the cited portions of Murphy teach that the selective oxide layer 46 that is

deposited on the bottom 44 of trench 34 has a thickness of 4000-5000 Å. *See, e.g.,* Figure 6 and Col. 5:1-20. Thus, Appellant submits that the problems identified by Lynch would not lead one of skill in the art to modify the Murphy reference as asserted by the Examiner. Moreover, the cited portions of Murphy teach that damage from the silicon etch process used to form trench 34 is removed by any one of conventional techniques, such as soft etch and annealing. *See, e.g.,* Col. 4:13-34. As is shown in Figure 2, the bottom 17 of Murphy's trench 10 does not have "surface roughness and/or sharp or irregular corners." Thus, one of skill in the art would not be motivated to modify Murphy to address problems that do not exist.

Moreover, the cited portions of the Murphy reference appear to teach away from using the process taught by Lynch. According to M.P.E.P. § 2141.02, a "prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." The cited portions of the Lynch reference teach that the final thickness of the trench-bottom oxide region 34 is approximately 1500 Å. *See, e.g.,* Col. 4:54-57. However, the Murphy reference teaches that the selective oxide layer 46 is deposited to a thickness of 4000-5000 Å with a final thickness of around 4000 Å (*see, e.g.,* Col. 5:1-44), and that select oxide 56 has a final depth of approximately 3500 Å (*see, e.g.,* Col. 7:4-9). The process taught by Lynch produces an oxide region that is significantly thinner than the select oxide of the Murphy reference. As a stated purpose of Murphy is to have a thick dielectric layer on the bottom of the trench (*see, e.g.,* the abstract), one of skill in the art would not be motivated to modify Murphy because such a modification would result in Murphy having a significantly thinner dielectric layer.

For at least these reasons, Appellant submits that the Examiner has provided no valid justification to combine Murphy and Lynch and has therefore failed to state a *prima facie* case of obviousness.

VIII. Conclusion

In view of the above, Appellant submits that the stated rejections are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,217)

1. A method of manufacturing a trench gate semiconductor device comprising the steps of: providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region; forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; etching the silicon at the base of the trench to form porous silicon at the base of the trench; and thermally oxidizing the device to oxidize the porous silicon at the bottom of the trench to form a plug at the base of the trench; and depositing conductive material within the trench to form a gate.

2. A method according to claim 1 further comprising, after the step of etching the trench, the step of lining the side walls of the trench with dielectric liner for preventing the side walls becoming porous during the step of forming porous silicon at the bottom of the trench.

4. A method according to claim 1 wherein the step of forming the trench includes providing a mask on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening.

5. A method according to claim 4 wherein the mask is an oxide hard mask.

6. A method according to claim 4 wherein the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom of the trench through the same mask used to define the trench.

8. A method according to claim 1 further comprising forming a source implant of first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.

9. A trench MOSFET comprising:

a drain region of first conductivity type;

a body region over the drain region;

a trench extending from a first major surface through the body region;

source regions of the first conductivity type laterally adjacent to the trench at the first major surface;

thermal gate oxide on the side walls of the trench;

a gate electrode in the trench insulated from the body region by the gate oxide;

characterised by a thick oxide plug formed of oxidized porous silicon at the base of the trench extending into the drain region.

10. A trench MOSFET according to claim 9 wherein the body region is of second conductivity type opposite to the first conductivity type.

APPENDIX OF PENDING CLAIMS NOT INVOLVED IN THE APPEAL
(S/N 10/538,217)

3. A method according to claim 1 wherein the step of oxidizing the device forms sidewall oxide on the sidewalls of the trench, the method further comprising the steps of etching away the oxide formed on the side wall oxide and of forming the gate oxide by thermal oxidation on the side wall before the step of depositing conductive material within the trench to form a gate.

7. A method according to claim 1 further comprising depositing a silicon plug in the trench wherein the step of etching the silicon at the bottom of the trench includes etching the silicon plug.

11. A method of manufacturing a trench gate semiconductor device, the method comprising:

providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region;

forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base;

etching the silicon at the base of the trench to form porous silicon at the base of the trench;

thermally oxidizing the device to oxidize the porous silicon at the base of the trench to form a plug at the base of the trench, wherein thermally oxidizing the device forms sidewall oxide on the sidewalls of the trench; and

depositing conductive material within the trench to form a gate.

12. The method of claim 11, further comprising etching away the sidewall oxide and forming a gate oxide by thermal oxidation on the sidewalls of the trench before depositing conductive material within the trench to form a gate.

13. The method of claim 11, wherein forming the trench includes providing a mask having an opening and on the first major surface and etching through the opening.

14. The method of claim 13, wherein the mask is an oxide hard mask.

15. The method of claim 13, wherein etching the silicon at the base of the trench to form porous silicon includes dry-etching the base of the trench through the same mask used to define the trench.

16. The method of claim 13, further comprising forming a source implant of the first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.